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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,714	12/31/2003	Ricardo E. Gonzalez	PA2683US	1388

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EXAMINER	
GEIB, BENJAMIN P	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 11/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,714	GONZALEZ ET AL.	
	Examiner	Art Unit	
	Benjamin P. Geib	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2006*.

2a)☒ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) *27-29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-26 have been examined.

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received on 07/24/2006.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Regarding claims 1 and 18, the phrase "whether or not a neighboring processor node comprises another software extensible device" renders the claims indefinite, as it is unclear as to whether or not the neighboring processor node is one of the previously mentioned "plurality of processing nodes". Since it is inherent that the processing nodes comprises a software extensible device due to the claimed description of the processing nodes (i.e. each processor node comprising...), the phrase "whether or not a neighboring processor node comprises software extensible device" will be interpreted as "a neighboring processor node that comprises a software extensible device" for the remainder of the examination.

6. All claims rejected by 35 U.S.C. 112, second paragraph, that have not been specifically addressed above are rejected on the basis of dependence.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1- 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Willis et al., U.S. Patent No. 5,999,734, (Herein referred to as Willis) in view of Arimilli et al., U.S. Patent No. 6,415,424 (Herein referred to as Arimilli).

9. Referring to claim 1, Willis has taught a system for processing applications, the system comprising:

a plurality of processor nodes with each processor node comprising:

a processing element *[processor; Fig. 1, component 1 or 2]* configured to execute at least one of the applications *[column 6, lines 36-43]*;

a software extensible device *[re-configurable logic block; Fig. 1, component 9]* configured to provide additional new instructions to a set of standard instructions for the processing element wherein the new instructions can be programmed by software *[column 6, lines 1-8, 24-29]*;

a communication interface *[shared memory interconnect and message interface; Fig. 1, components 7 & 10]* configured to communicate with other processor nodes using different communication protocols based on a

neighboring processor node that comprises software extensible device and whether the neighboring processor node is on a separate node or on a same node *[wherein two nodes (components 11 and 12) are shown in Fig. 1; column 5, lines 4-8, 31-54]*; and

a plurality of links interconnecting the processor nodes *[links connecting the message interfaces (Fig. 1, components 10) to the message interconnect (Fig. 1, component 13)]*.

Willis does not disclose expressly that the nodes (i.e. components 11 and 12) are on different chips.

Arimilli discloses processing nodes are on different chips *[See Fig. 2B; column 5, lines 48-55]*.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the system of Willis to have the nodes (components 11 and 12) on different chips. In doing so, the communication interface would be configured to communicate with other processor nodes using different communications protocols based on whether the neighboring processor node is on a separate chip or on a same chip (i.e. the message interface would be used when communicating to a processor node on a separate chip, but not when communicating to a processor on a same chip).

The suggestion/motivation for doing so would have been that the system cost is reduced.

Referring to claim 2, Willis and Arimilli have taught the system of claim 1.

Willis and Arimilli have not explicitly taught that each one of the processor nodes is on a separate chip.

However, Examiner takes Official Notice that having each processor node on a separate chip is conventional and well-known.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Willis and Arimilli to have each processor node on a separate chip since doing so would reduce system cost..

10. Referring to claim 3, Willis and Arimilli have taught the system of claim 1, wherein at least some of the processor nodes are on the same chip *[Willis; See Fig.1]*.

11. Referring to claim 4, Willis and Arimilli have taught the system of claim 1 wherein the plurality of the processor nodes are configured in an array *[Willis;; See Fig.1]*.

12. Referring to claim 5, Willis and Arimilli have taught the system of claim 1wherein the software extensible device comprises an instruction set extension fabric *[Willis; The software extensible device (i.e. re-configurable logic block) comprises a fabric of re-configurable logic devices (See Fig. 2) that extend the instruction set; column 6, lines 1-8]*.

13. Referring to claim 6, Willis and Arimilli have taught the system of claim 1 wherein the software extensible device comprises a programmable logic device *[Willis; The software extensible device (i.e. re-configurable logic block) is a logic device that is programmable; column 5, lines 31-53]*.

14. Referring to claim 7, Willis and Arimilli have taught the system of claim 1 wherein the communication interface is configured to communicate using shared memory *[Willis; column 5, lines 20-30]*.

15. Referring to claim 8, Willis and Arimilli have taught the system of claim 1 wherein the communication interface is configured to communicate using message passing *[Willis; column 5, lines 4-8]*.

16. Referring to claim 9, Willis and Arimilli have taught the system of claim 1 wherein the communication interface is configured to communicate using channels between the processor nodes *[Willis; Since the processor nodes communicate with each other there are inherently channels of communication between the processor nodes; See Fig. 1; column 5, lines 4-8]*.

17. Referring to claim 10,

Willis and Arimilli have taught the system of claim 9.

Willis and Arimilli have not explicitly taught that the communication interface is configured to perform time division multiplexing using the channels between the processor nodes.

However, Examiner takes Official Notice that communication interfaces configured to perform time division multiplexing using the channels between the processor nodes are conventional and well-known.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Willis and Arimilli so that the communication interface is configured to perform time division multiplexing using the

channels between the processor nodes since doing so allows a single transmission path to be shared by multiple signals.

18. Referring to claim 11,

Willis and Arimilli have taught the system of claim 9.

Willis and Arimilli have not explicitly taught that the communication interface is configured to perform spatial division multiplexing using the channels between the processor nodes.

However, Examiner takes Official Notice that communication interfaces configured to perform spatial division multiplexing using the channels between the processor nodes are conventional and well-known.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Willis and Arimilli so that the communication interface is configured to perform spatial division multiplexing using the channels between the processor nodes since doing so increases data transmission speed.

19. Referring to claim 12, Willis and Arimilli have taught the system of claim 1 wherein the communication interface comprises a processor network interface *[Willis; The message interface interfaces a network of processors; See Fig. 1]*.

20. Referring to claim 13,

Willis and Arimilli have taught the system of claim 1.

Willis and Arimilli have not explicitly taught that the communication interface comprises a processor network switch.

However, Examiner takes Official Notice that communication interfaces comprising a processor network switch are conventional and well-known.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Willis and Arimilli so that the communication interface comprises a processor network switch since doing so advantageously allows the connection of multiple network segments.

21. Referring to claim 14, Willis and Arimilli have taught the system of claim 1 wherein the communication interface comprises a standard input/output interface *[Willis; The message interface implements the IEEE standard 1596 protocol and, therefore, comprises a standard input/output interface; column 5, lines 4-9. Furthermore, any processor communication interface that implements input/output is inherently a standard input/output interface since it is the standard input/output interface for the system].*

22. Referring to claim 15, Willis and Arimilli have taught the system of claim 1 wherein the communication interface comprises an interface module configured to communicate between processor nodes on different chips *[Willis; The message interface is configured to communicate between processor nodes on different chips since whether or not the processor nodes are on different chips does not affect the communication interface; See Fig. 1; column 5, lines 4-8].*

23. Referring to claim 16,

Willis and Arimilli have taught the system of claim 1.

Willis and Arimilli have not explicitly taught that the communication interface comprises a multiplexer/demultiplexer.

However, Examiner takes Official Notice that communication interfaces comprising a multiplexer/demultiplexer are conventional and well-known.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Willis and Arimilli so that the communication interface comprises a multiplexer/demultiplexer since doing so allows the combination of multiple data streams into a single data stream that can be advantageously transmitted over a single transmission link.

24. Referring to claim 17, Willis and Arimilli have taught the system of claim 1 wherein at least one of the processor nodes is different from the other processor nodes *[Willis; The two processing nodes are two distinct devices and are, therefore, different; See Fig. 1]*.

25. Referring to claim 18, Willis has taught a method for a system with multiple processor nodes, the method comprising:

executing an application in at least one processing element *[processor; Fig. 1, component 1 or 2]* in a plurality of the processor nodes *[column 6, lines 36-43]*;

providing an additional new instruction to a set of standard instructions for the processing element using at least one software extensible device *[re-configurable logic block; Fig. 1, component 9]* in the plurality of the processor nodes wherein the new instructions can be programmed by software *[column 6, lines 1-8, 24-29]*;

communicating between the processor nodes using at least one communication interface *[shared memory interconnect and message interface; Fig. 1, components 7 & 10]* in a plurality of the processor nodes using different communications protocols based

on a neighboring processor node that comprises a software extensible device and whether the neighboring processor node is on a separate node or on a same node *[wherein two nodes (components 11 and 12) are shown in Fig. 1; column 5, lines 4-8, 31-54].*

Willis does not disclose expressly that the nodes (i.e. components 11 and 12) are on different chips.

Arimilli discloses processing nodes are on different chips *[See Fig. 2B; column 5, lines 48-55].*

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the method of Willis to have the nodes (components 11 and 12) on different chips. In doing so, the communication interface would be configured to communicate with other processor nodes using different communications protocols based on whether the neighboring processor node is on a separate chip or on a same chip (i.e. the message interface would be used when communicating to a processor node on a separate chip, but not when communicating to a processor on a same chip).

The suggestion/motivation for doing so would have been that the system cost is reduced.

26. Referring to claim 19, given the similarities between claim 7 and claim 19 the arguments as stated for the rejection of claim 7 also apply to claim 19.

27. Referring to claim 20, given the similarities between claim 8 and claim 20 the arguments as stated for the rejection of claim 8 also apply to claim 20.

28. Referring to claim 21, given the similarities between claim 9 and claim 21 the arguments as stated for the rejection of claim 9 also apply to claim 21.

29. Referring to claim 22, given the similarities between claim 10 and claim 22 the arguments as stated for the rejection of claim 10 also apply to claim 22.

30. Referring to claim 23, given the similarities between claim 11 and claim 23 the arguments as stated for the rejection of claim 11 also apply to claim 23.

31. Referring to claim 24, Willis and Arimilli have taught the method of claim 18 further comprising compiling the application *[Willis; column 6, lines 36-43]*.

32. Referring to claim 25, Willis and Arimilli have has taught the method of claim 18 further comprising loading the application into one of the plurality of the processor nodes *[It is inherent that in order for an application to be executed in a processor node the application is loaded into the node]*.

33. Referring to claim 26,

Willis and Arimilli have taught the method of claim 18.

Willis and Arimilli have not explicitly taught configuring one of the processor nodes to select between an interface module and a standard input/output interface based on a neighboring device.

However, Examiner takes Official Notice that configuring processor nodes to select between an interface module and a standard input/output interface based on a neighboring device is conventional and well-known.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Willis and Arimilli so that a processor node is configured to select between an interface module and a standard input/output interface based on a neighboring device since doing so would allow communication between the neighboring device and the processor node.

Response to Arguments

34. Applicants arguments filed on July 24, 2006, have been fully considered but they are not found persuasive.

35. Applicant argues the novelty/rejection of claims 1-26 on pages 10-14 of the remarks, in substance that:

> "Thus, the re-configurable logic block of Willis is not configured to accept additional new instructions and may implement only reserved instructions" (1st paragraph on page 11)
>
> "Thus, Willis does not teach a software extensible device configured to provide additional new instructions to a set of standard instructions for the processing element wherein the new instructions can be programmed by software, as recited in amended claim 1." (1st paragraph on page 12)
>
> "Thus, Willis does not teach or suggest using different communication protocols based on whether or not a neighboring processor node comprises another software extensible device and whether the neighboring processor node is on a separate chip or on a same chip, as recited in amended claim 1." (3rd paragraph on page 13)

These arguments are not found persuasive for the following reasons:

In response to applicant's argument that Willis does not provide additional new instruction, the examiner notes that while the instruction op-codes of Willis are reserved from the instruction set encodings of the processor, the instructions provided using these op-codes are new additional instructions to the set of standard instructions for the

processor since these instructions are not defined as part of the standard instruction for the processor (column 6, lines 1-22).

The applicant asserts that the instructions of Willis are not programmed by software. It is noted that since the reconfigurable logic block (which executes the additional instructions) may be reconfigured through software (column 6, lines 23-28), the instructions executed by the reconfigurable logic block are programmed by software.

36. Applicant's arguments with respect to using different communication protocols based on whether or not a neighboring processor node comprises another software extensible device and whether the neighboring processor node is on a separate chip or on a same chip have been considered but are moot in view of the new grounds of rejection.

37. Applicant argues the Examiner's taking of Official Notice with regards to claims 2, 3, 10, 11, 13, 16, 22, 23, and 26 on pages 14-20 of the remarks and requests that the Examiner provide references indicating that the element taken Official Notice of were conventional and well-known at the time of the application. The Examiner provides the following references as extrinsic evidence that the elements taken Official Notice of were conventional and well-known at the time of the application:

Regarding claims 2 and 3, see Arimilli et al., U.S. Patent No. 6,415,424 (column 5, lines 21-35).

Regarding claims 10, 11, 13, 22, and 23, see Lee, "A Virtual Bus Architecture for Dynamic Parallel Processing" (section B);

Regarding claims 16 and 26, see Noakes et al., U.S. Patent No. 5,847,578 (See Fig. 4; column 3, lines 19-41);

Conclusion

38. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

39. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin P. Geib whose telephone number is (571) 272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Benjamin P Geib
Examiner
Art Unit 2181

KIM HUYNH
SUPERVISORY PATENT EXAMINER

10/30/06